WHAT IS CLAIMED IS:

1. A delay locked loop (DLL) circuit for phase matching of a periodic input signal, comprising:

a variable delay unit;

a delay element;

a regulation unit having a regulation device for setting an input signal delay in the delay unit and a comparator unit for generating a phase signal in each signal cycle, wherein the state of the phase signal indicates a lead-lag relation between the input signal and a delayed signal which has been delayed by the variable delay unit and the delay element, the phase signal is provided to the regulation device during a steady-state operating phase, and the regulation device adjusts the delay of the variable delay unit during an initial transient phase until a change in the sate of the phase signal is detected indicating a change in the lead-lag relation between the input signal and the delayed signal; and

a filter circuit for providing a filtered phase signal to the regulation device during the initial transient phase, wherein the filter circuit changes the state of the filtered phase signal to the state of the phase signal only when a different state of the phase signal with respect to the state of the filtered phase signal has been detected for a predetermined number of successive signal cycles.

2. The DLL circuit of claim 1, wherein the predetermined number of successive signal cycles is variable.

3. The DLL circuit of claim 2, wherein the predetermined number of successive signal cycles is chosen such that the signal delay between the input signal and the delayed signal is less than the multiple of the signal cycle time by the predetermined number.

4. The DLL circuit of claim 1, wherein the predetermined number of successive signal cycles is 4.

5. The DLL circuit of claim 1, wherein the regulation device varies the delay of the variable delay unit incrementally, with the increments being greater during the initial transient phase than during the steady-state operating phase.

6. The DLL circuit of claim 1, wherein the regulation device increases the delay of the variable delay unit incrementally during the initial transient phase until a change in the phase signal indicates a change from the input signal lagging the delayed signal to the input signal leading the delayed signal.

7. The DLL circuit of claim 1, wherein the filter circuit comprises a shift register having a predetermined number of register stores, the phase signal is applied to an input of the shift register, and the filtered phase signal changes state only when a different state than the state of the phase signal is stored in all of the shift registers.

8. The DLL circuit of claim 7, wherein the filter circuit comprises an SR flip-flop having a set input connected to the output of an AND gate and a reset input connected to the output of a NOR gate, with the outputs of the register stores in the shift register connected to inputs of the AND gate and to inputs of the NOR gate.

9. A method for phase matching of a periodic input signal during an initial transient phase, comprising:

generating a phase signal with each cycle of the input signal, wherein a state of the phase signal indicates whether the input signal is leading or lagging a delayed signal;

varying a delay of the delayed signal based on the state of the phase signal, wherein the delay of the delayed signal is varied incrementally during the initial transient phase; and

transitioning from the initial transient phase to a steady-state operating phase when a change in the phase signal indicates a phase angle of 0° between input and delayed signals, wherein the phase signal is filtered during the initial transient phase and the state of the filtered phase signal changes only when a different state of the

phase signal with respect to the state of the filtered phase signal has been detected for a predetermined number of successive signal cycles.

10. The method of claim 9, wherein the delay of the delayed signal during the initial transient phase is increased incrementally until it is identified that the input signal has changed from an identified lag to a lead with respect to the delayed signal.

11. The method of claim 9, comprising:

varying the delay of the delayed signal using a first increment during the initial transient phase; and

varying the delay of the delayed signal using a second increment during the steady-state operating phase, wherein the second increment is larger than the first increment.

12. The method of claim 9, wherein the state of the filtered phase signal changes only when a different state of the phase signal with respect to the state of the filtered phase signal has been detected for a predetermined number of successive signal cycles, wherein the predetermined number of successive signal cycles is chosen such that the signal delay between the input signal and the delayed signal is less than the multiple of the signal cycle time by the predetermined number.

13. The method of claim 9, comprising generating the filtered phase signal by logically ANDing shift register outputs indicative of the phase signal during multiple successive signal cycles.

14. The method of claim 13, comprising generating the filtered phase signal by logically NORing the shift register outputs.

15. The method of claim 14, comprising setting an SR flip-flop with a signal indicative of the logical ANDing and resetting the SR flip-flop with a signal indicative of the logical NORing.

16. An integrated circuit (IC) device, comprising:

a clock signal line for carrying a clock signal; and

a delay locked loop (DLL) circuit for compensating for propagation time delay of the clock signal, the DLL circuit having

a delay unit and variable delay element for generating a delayed signal from the clock signal,

a regulation circuit for adjusting the variable delay element, and a comparator unit for generating a phase signal in each signal cycle, wherein the state of the phase signal indicates a lead-lag relation between the clock signal and the delayed signal, the phase signal is provided to the regulation device during a steady-state operating phase, and the regulation device adjusts the delay of the variable delay unit during an initial transient phase until a change in the sate of the phase signal is detected indicating a change in the lead-lag relation between the clock signal and the delayed signal, and

a filter circuit for providing a filtered phase signal to the regulation device during the initial transient phase, wherein the filter circuit changes the state of the filtered phase signal to the state of the phase signal only when a different state of the phase signal with respect to the state of the filtered phase signal has been detected for a predetermined number of successive clock signal cycles.

17. The IC device of claim 16, wherein the predetermined number of successive signal cycles is chosen such that the signal delay between the clock signal and the delayed signal is less than the multiple of the clock signal cycle time by the predetermined number.

18. The IC device of claim 16, wherein the regulation device of the DLL varies the delay of the variable delay unit incrementally, with the increments being greater during the initial transient phase than during the steady-state operating phase.

19. The IC device of claim 16, wherein the regulation device of the DLL increases the delay of the variable delay unit incrementally during the initial transient phase

until a change in the phase signal indicates a change from the clock signal lagging the delayed signal to the clock signal leading the delayed signal.

20. The IC device of claim 16, wherein the filter circuit of the DLL comprises a shift register having a predetermined number of register stores, wherein the phase signal is applied to an input of the shift register and the filtered phase signal changes state only when a different state than the state of the phase signal is stored in all of the shift registers.